Electronics for the camera of the First G-APD Cherenkov Telescope (FACT) for ground based gamma-ray astronomy

2012 JINST 7 C01073

(http://iopscience.iop.org/1748-0221/7/01/C01073)

Jinst
PUBLISHED BY IOP PUBLISHING FOR SISSA

RECEIVED: *October 31, 2011*
ACCEPTED: *December 20, 2011*
PUBLISHED: *January 19, 2012*

TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS 2011,
26–30 SEPTEMBER 2011,
VIENNA, AUSTRIA

Electronics for the camera of the First G-APD Cherenkov Telescope (FACT) for ground based gamma-ray astronomy

H. Anderhub,[a] M. Backes,[b] A. Biland,[a] A. Boller,[a] I. Braun,[a] T. Bretz,[c] V. Commichau,[a] L. Djambazov,[a] D. Dorner,[a,d] C. Farnier,[d] A. Gendotti,[a] O. Grimm,[a] H.P. von Gunten,[a] D. Hildebrand,[a] U. Horisberger,[a] B. Huber,[a,f] K.-S. Kim,[a,g] J.-H. Köhne,[b] T. Krähenbühl,[a] B. Krumm,[b] M. Lee,[a,g] J.-P. Lenain,[d] E. Lorenz,[a,h] W. Lustermann,[a] E. Lyard,[d] K. Mannheim,[e] M. Meharga,[d] D. Neise,[b] F. Nessi-Tedaldi,[a] A.-K. Overkemping,[b] F. Pauss,[a] D. Renker,[a,i] W. Rhode,[b] M. Ribordy,[c] R. Rohlfs,[d] U. Röser,[a] J.-P. Stucki,[a] J. Thaele,[b] O. Tibolla,[e] G. Viertel,[a] P. Vogler,[a,1] R. Walter,[d] K. Warda[b] and Q. Weitzel[a]

[a]*Institute for Particle Physics, ETH Zurich,*
Schafmattstr. 20, 8093 Zurich, Switzerland
[b]*TU Dortmund University,*
Otto-Hahn-Str. 4, 44227 Dortmund, Germany
[c]*École Polytechnique Fédérale de Lausanne,*
Laboratory for High Energy Physics, 1015 Lausanne, Switzerland
[d]*ISDC Data Center for Astrophysics, University of Geneva,*
Chemin d'Ecogia 16, 1290 Versoix, Switzerland
[e]*University of Würzburg,*
Am Hubland, 97074 Würzburg, Germany
[f]*University of Zurich,*
8057 Zurich, Switzerland
[g]*Kyungpook National University, Center for High Energy Physics,*
702-701 Daegu, Korea
[h]*Max-Planck-Institut für Physik,*
80805 Munich, Germany
[i]*Technische Universität München,*
85748 Garching, Germany

E-mail: patrick.vogler@phys.ethz.ch

---

[1] Corresponding author.

doi:10.1088/1748-0221/7/01/C01073

ABSTRACT: Within the FACT project, we construct a new type of camera based on Geiger-mode avalanche photodiodes (G-APDs). Compared to photomultipliers, G-APDs are more robust, need a lower operation voltage and have the potential of higher photon-detection efficiency and lower cost, but were never fully tested in the harsh environments of Cherenkov telescopes. The FACT camera consists of 1440 G-APD pixels and readout channels, based on the DRS4 (Domino Ring Sampler) analog pipeline chip and commercial Ethernet components. Preamplifiers, trigger system, digitization, slow control and power converters are integrated into the camera.

KEYWORDS: Photon detectors for UV, visible and IR photons (solid-state) (PIN diodes, APDs, Si-PMTs, G-APDs, CCDs, EBCCDs, EMCCDs etc); Gamma telescopes; Cherenkov and transition radiation; Particle detectors

2012 JINST 7 C01073

Contents

1 Introduction

Since the discovery of the Crab Nebula as a TeV γ-ray source [1], Imaging Atmospheric Cherenkov Telescopes (IACTs) have been very successful in detecting galactic and extragalactic very high energy (50 GeV–100 TeV) γ-ray sources [2]. The key component of every IACT is a pixelated camera with the temporal resolution to detect the Cherenkov light flashes from air showers. These light flashes have a duration of about 1 - 5 ns and are very faint — for a 1 TeV primary γ, there are about 100 Cherenkov photons per square meter. This requires a high camera sensitivity. Cherenkov photons are emitted in the visible and near ultraviolet range. Until now, all IACT cameras were based on photomultiplier tubes (PMTs). Since several years so-called G-APDs (Geiger-mode avalanche photodiodes) [3], which are solid state photodetectors became available. These G-APDs are auspicious compared to the PMTs used up to now: G-APDs promise a higher photon-detection efficiency, they allow single photon resolution and are rather insensitive to bright light. The required bias voltage is much lower, on the order of 70 V instead of the kVs required by PMTs. Furthermore, G-APDs are mechanically more robust, and there are no known aging effects. And in contrast to PMTs, G-APDs are insensitive to magnetic fields. The G-APDs used in the FACT camera have a dark count rate below 10 MHz [4] per pixel. A small-scale prototype of a G-APD based camera has successfully been used to record cosmic ray induced air showers [5]. Nevertheless a full-scale camera has not yet shown its performance in Cherenkov astronomy. Therefore, the conclusive proof that G-APDs are a viable replacement for PMTs in future IACT cameras[1] is still missing. In this proceeding, the trigger and data-acquisition electronics of the FACT camera, the first full-scale G-APD based IACT camera, is presented.

---

[1] As for the planned Cherenkov Telescope Array [6]

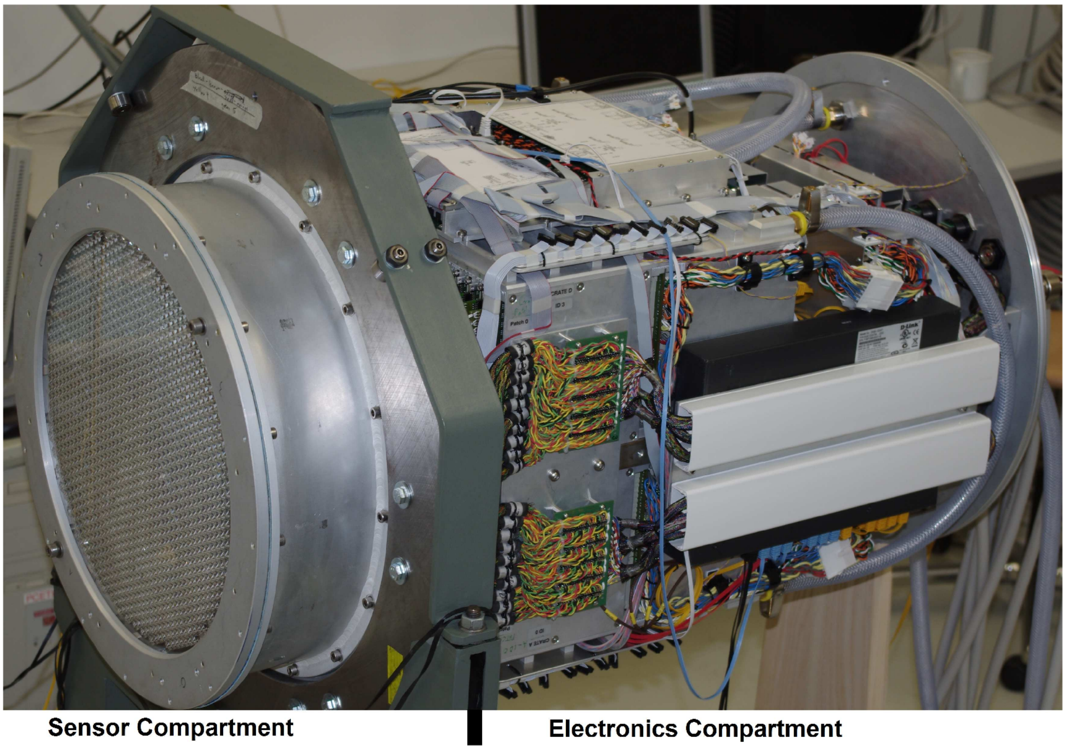

Figure 1. The FACT camera in the laboratory during the assembly- and test phase: On the left, the sensor compartment and the front window can be seen. The electronics compartment is shown on the right.

2 General layout of the FACT camera

The two main parts of the FACT camera are the sensor compartment with the solid parabolic light concentrators [7, 8] and the G-APDs [3, 4] and the electronics compartment with the trigger- and readout electronics. These two compartments are indicated in figure 1, which shows the FACT camera during assembly and testing. The FACT camera comprises 1440 pixels and the same number of readout channels. In order to avoid heating-up the G-APDs, the sensor compartment is thermally decoupled from the electronics compartment. This allows for an operation without active cooling of the G-APDs. Temperature sensors near the G-APDs provide the necessary basic information to adjust the bias voltage (see subsection 2.7) of the G-APDs.

The pixels of the FACT camera have a hexagonal shape and a pitch of 9.5 mm, which corresponds to an angle of 0.11 degree field of view per pixel. The front window has a diameter of about 40 cm, making a field of view of approximately 4.5 degree. The readout- and trigger electronics is subdivided into four crates containing ten preamplifier- trigger unit- and digitizer boards each. The preamplifier- trigger unit- and digitizer boards have 36 channels each, resulting in 40 boards of each kind. An overview of the FACT camera electronics is given in the block diagram in figure 2.

In addition to the four crates of trigger- and readout electronics the FACT camera also comprises one trigger master board, two fast signal distribution boards, a slow control board and power converters. The waste heat of the electronics is removed by means of water cooling. The shutter of the FACT camera is equipped with a light pulser system for functional tests during daytime. A

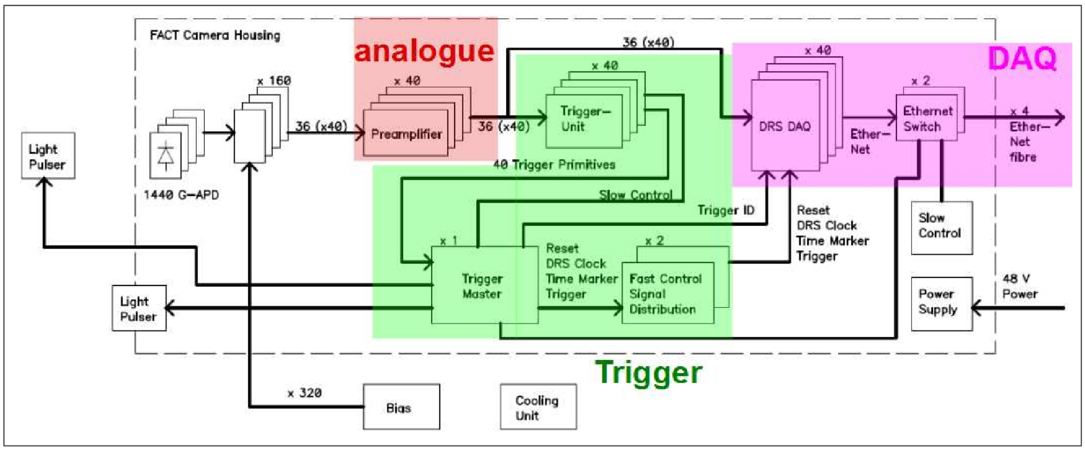

Figure 2. Schematic diagram of the FACT camera electronics.

second lightpulser for feedback and calibration purposes (see [9]) is to be placed at the center of the telescope's mirror dish. Beside this lightpulser and the cooling unit, the only component not integrated in the FACT camera is the bias voltage supply (see subsection 2.7).

2.1 Preamplifier

The preamplifier board comprises 36 channels i.e. four trigger patches. It performs a current to voltage conversion and an amplification of the signal coming from the G-APD. A low noise RF transistor in grounded-base circuit configuration provides current buffering. Two parallel 390 Ω resistors convert the current signal into an voltage pulse and the following operational amplifier stage provides the necessary signal gain. The amplified signals are then fed to the corresponding data-acquisition board (see subsection 2.3) for digitization. The preamplifier board also performs a patch-wise summation of the nine signals of each trigger patch, and a cable-based clipping limits the pulse length to 10 ns. After the summation, the trigger threshold provided by the trigger unit (see subsection 2.2) is applied and the resulting comparator signal is then fed to the trigger unit.

2.2 Trigger unit

The trigger unit sets a discriminator threshold to every trigger patch consisting of nine pixels. The pixels of the FACT camrea are arranged on a hexagonal grid (honeycomb), and the geometrical arrangement of the pixels comprising a trigger patch can be seen in figure 3. The discriminator signals from all four patches are collected by the trigger unit and the corresponding rates are monitored (counted) in an on-board XILINX XC3S400AN FPGA (Field-programmable Gate Array). This FPGA is also controlling the DAC (digital-to-analogue converter) used to set the discriminator thresholds. The patch-wise trigger signals are fed to an 'n-out-of-4' logic generating a single signal that serves as trigger primitive. This trigger primitive signal is fed to the trigger master board (see subsection 2.4), and its rate is monitored on board in the same manner as the four discriminator signals. In addition, the trigger unit, together with the preamplifier, provides the possibility to exclude single pixels from a trigger patch. This is foreseen do deal with noisy or defective pixels as well as with stars in a trigger patch. The trigger unit features an RS-485 bus to provide a communication

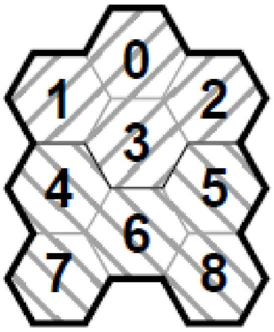

Figure 3. A trigger patch of the FACT camera consisting of nine pixels.

link to the trigger master for slow-control purpose such as setting thresholds (i.e. DAC values) and reading out rates. Mechanically, the trigger unit is designed as a mezzanine board sitting on the preamplifier board, while the trigger primitive signal is fed to the trigger master by means of a coaxial cable.

2.3 Data-acquisition board

The data-acquisition of the FACT camera is based on the DRS4 (Domino Ring Sampler) [10] analogue pipeline chip designed at the Paul Scherrer Institute in Switzerland. The DRS4 chip is a switched capacitor array with 9 channels and 1024 storage cells per channel. It can be operated at sampling rates from 700 MSPS to 5 GSPS. For FACT, a default sampling rate of 2 GSPS is planned. After the DRS4 chip, an external analogue to digital converter is required, which is, in our case operated with a sampling clock of 20 MHz. The dynamic range (effective number of bits) is 11.5 bits — enough to allow for a single photoelectron resolution assuming a maximum range of about 200 photoelectrons per channel. The DRS4 chip allows the region of interest (ROI) i.e. the number of slices to be read out and subsequently digitized, to be set individually for each channel. Every board features four DRS4 chips and a 100 Mbps Fast Ethernet interface (Wiznet W5300) for data readout and slow control purpose. On every DAQ board the control logic is implemented in a Xilinx XC3SD3400A FPGA. In order to receive the trigger-IDs from the trigger master (see subsection 2.4), every board is equipped with a dedicated RS-485 bus. The trigger-ID is sent to the data-acquisition computer together with the data.

2.4 Trigger master

The FACT Trigger master collects the 40 trigger primitives from the trigger units to generate the trigger- and the time marker signal. Furthermore it generates the reference clock for the DRS4 chips (see subsection 2.3) and the resets signals, as well as a trigger-ID. The trigger-ID consists of a consecutive 32 bit number of the triggers and a two byte trigger-type information encoding the different trigger types: physics trigger, internal or external lightpulser, pedestal trigger, external trigger input. The trigger-ID is sent to the data-acquisition boards over a dedicated RS-485 bus. The trigger master board also acts as a slow control master for the trigger units, controlling them via an RS-485 bus. For the timing calibration of the DRS4 domino ring sampling chip, the trigger master provides a timing calibration signal on the time marker line. The trigger master itself is controlled via its Wiznet W5300 100 Mbit Fast Ethernet interface. The digital logic functions of the trigger master are implemented in an Xilinx XC3SD3400A FPGA, while a clock conditioner (National Semiconductor LMK03000) is used to generate the DRS4 reference clock.

2.5 Clock and trigger distribution

Inside the FACT camera, the following fast control signals from the trigger master have to be distributed: trigger, DRS clock, and time marker. Signal distribution is done using the LVDS standard and RJ-45 cables. Two signal distribution boards are used, comprising two ten-fold fan-outs (ON Semiconductor MC100LVEP111) each and for every signal. From there, the fast control signals are fed to the data-acquisition board using RJ-45 cables fabricated by the company WIREWIN with a custom length of 30 cm.

2.6 Ethernet interface

The whole data-readout as well as the slow control functions of the FACT camera are done via Ethernet. Two commercial gigabit Ethernet switches are integrated into the FACT camera in order to provide the necessary network connections. From these Ethernet switches there are four Gigabit Ethernet links to the DAQ computer. These Gigabit links use optical fibers. The measured data rate exceeds 300 MB/s, allowing to operate the camera with up to 1 kHz trigger rate.[2]

2.7 Power- and Bias voltage supply

The FACT camera is powered by an external 48 V DC power supply. A set of power converters (VICOR DC-DC Converter) inside the FACT camera provides all the necessary low voltage supplies by converting down the 48 V. The total power consumption is of the order of 600 W. In contrast to the low voltage supply, the bias supply is not integrated into the camera and comprises 320 channels plus spares. Each trigger patch of nine G-APDs is subdivided into two bias patches of four respectively five G-APDs connected to the same bias channel. Connecting several G-APDs to one bias supply channel required grouping the G-APDs according to their individual breakdown voltages. The bias voltages of the G-APDs is adjusted according to temperatures measured in the sensor compartment.

3 First results, summary and outlook

The whole trigger- and DAQ electronics has been fully commissioned and installed in the FACT camera. Various tests and measurements have been done in the laboratory where the following performance has been established: The electronic noise of the readout electronics is about 1.8 mV and therefore significantly lower than the signal of a single photoelectron, which is about 10 mV. Single and double photoelectron events can be seen in figure 4. Therefore, single photoelectron resolution is clearly established.

Full-scale reading corresponds to about 200 photoelectrons per pixel. With a readout of the full region of interest (ROI), a read-out rate of 60–80 Hz has been reached during laboratory tests.

---

[2] In connection with a foreseen software trigger

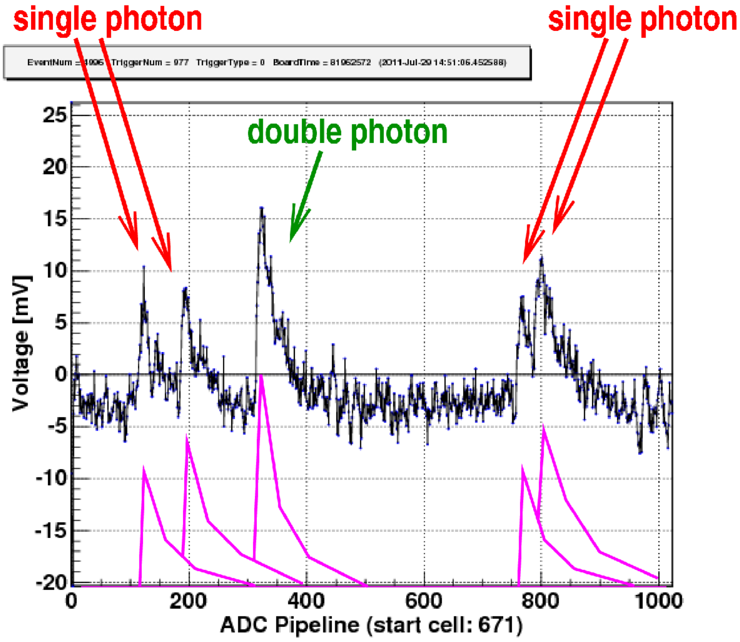

Figure 4. Single photoelectrons and a double photoelectron recorded with the DAQ of the FACT camera.

Figure 5. The FACT camera mounted on the telescope at the Roque de los Muchachos observatory on La Palma, Canary Islands, Spain.

Smaller ROIs result in a correspondingly higher maximum trigger rate. In the trigger system, the noise allows a threshold as low as about 20 photoelectrons per trigger patch, corresponding to a mean of about two photoelectrons per pixel. In October 2011 the FACT camera has been shipped to La Palma, Canary Islands, Spain, where it has been mounted on a refurbished HEGRA telescope on the site of the observatory on the Roque de los Muchachos. The mounted camera can be seen in figure 5. Commissioning on La Palma is (as by October 2011) still in progress.

Acknowledgments

The important contributions from ETH Zurich grant ETH-10.08-2 as well as the funding of novel photo-sensor research by the German BMBF Verbundforschung are gratefully acknowledged. We also thank the Instituto de Astrofisica de Canarias allowing us to operate the telescope at the Observatorio del Roque de los Muchachos on La Palma, and the Max-Planck-Institut für Physik for providing us with the mount of the former HEGRA CT3 telescope.

References

[1] T.C. Weekes et al., *Observation of TeV gamma rays from the Crab nebula using the atmospheric cerenkov imaging technique*, *Astrophys. J.* **342** (1989) 379.

[2] F. Aharonian et al., *High energy astrophysics with ground-based gamma ray detectors*, *Rep. Prog. Phys.* **71** (2008) 096901.

[3] D. Renker and E. Lorentz, *Advances in solid state photon detectors*, 2009 *JINST* **4** P04004.

[4] Hamamatsu Photonics K.K., *MPPC Multi-Pixel Photon Counter* (2008).

[5] FACT collaboration, H. Anderhub et al., *A novel camera type for very high energy gamma-ray astronomy based on Geiger-mode avalanche photodiodes*, 2009 *JINST* **4** P10010.

[6] *CTA — Cherenkov Telescope Array*, http://www.cta-observatory.org (2011).

[7] FACT collaboration, I. Braun et al., *Solid light concentrators for Cherenkov astronomy*, in the proceedings of the 31st *International Cosmic Ray Conference*, July 7–15, Łódź, Poland (2009).

[8] B. Huber et al., *Solid light concentrators for small-sized photosensors used in Cherenkov telescopes*, in the proceedings of the 32nd *International Cosmic Ray Conference*, August 11–18, Beijing, China (2011).

[9] T. Krähenbühl et al., *Calibration of the first G-APD Cherenkov telescope camera*, in the proceedings of the 32nd *International Cosmic Ray Conference*, August 11–18, Beijing, China (2011).

[10] S. Ritt, *Design and performance of the* 6 *GHz waveform digitizing chip DRS4*, *IEEE Nucl. Sci. Symp. Conf. Rec.* (2009) 1512.